

Progress in Scaling of Microelectronics and Future Trends

Robert H. Dennard, IBM Fellow

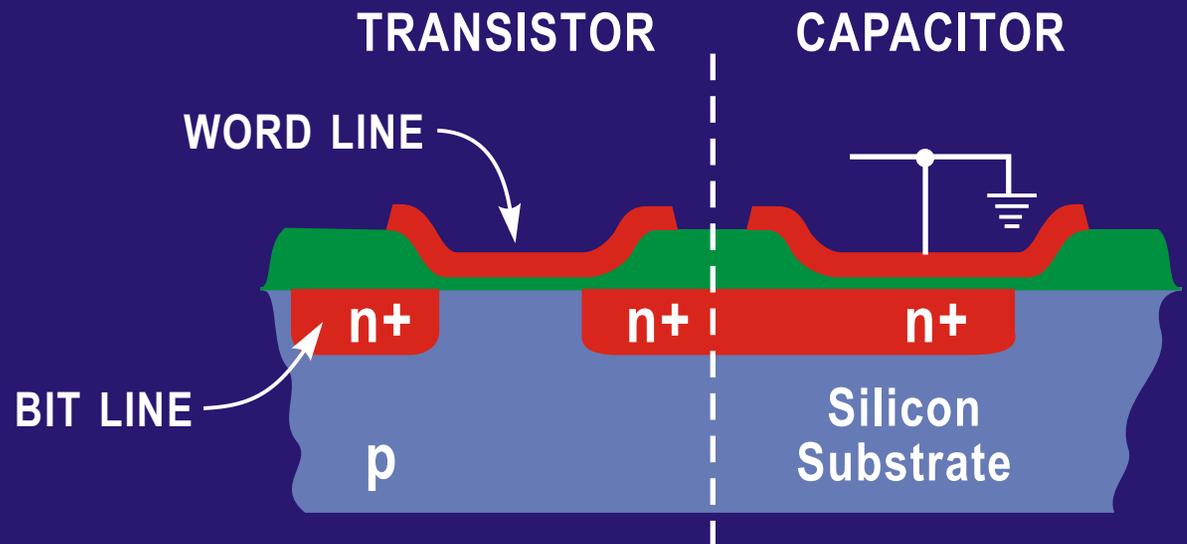
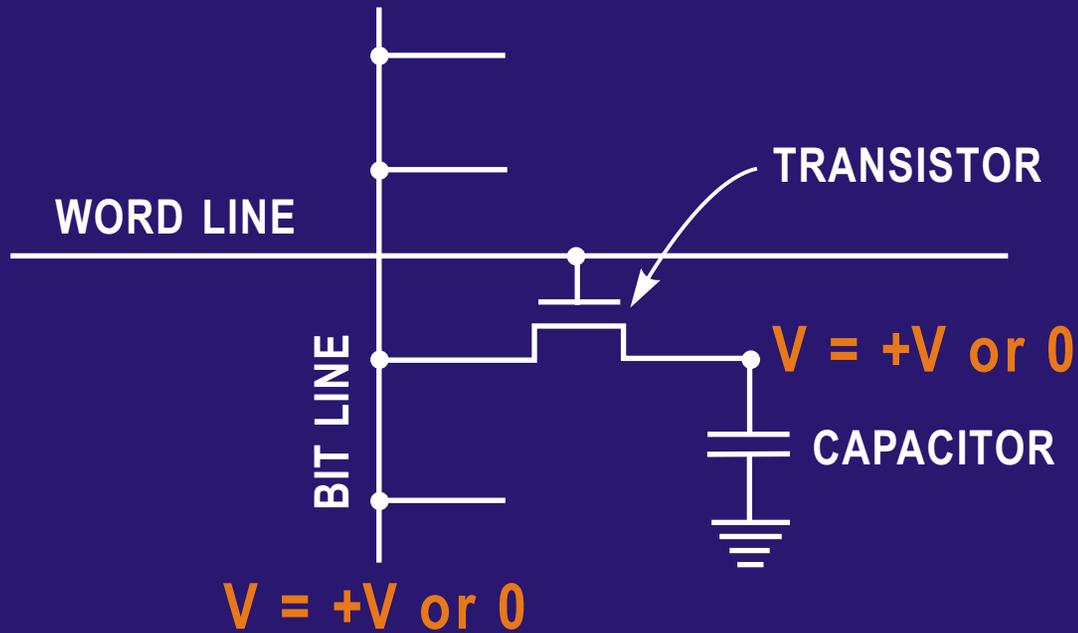
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Chronology of the Microelectronics Era

- **Phase I, 1926-1957, Discovery**
 - Rudimentary Semiconductor Device Concepts
- **Phase II, 1958-1968, Basic Technology and Transistor Innovation**
 - Early Integrated Circuits
 - Control of Silicon Surface and Insulators
- **Phase III, 1969- , Integrated Circuit Production**
 - Commercial Applications
 - Continuous Evolution of Capability

(After Prof. C.T. Sah)

ONE - TRANSISTOR DRAM MEMORY CELL



STORED-CHARGE CELL

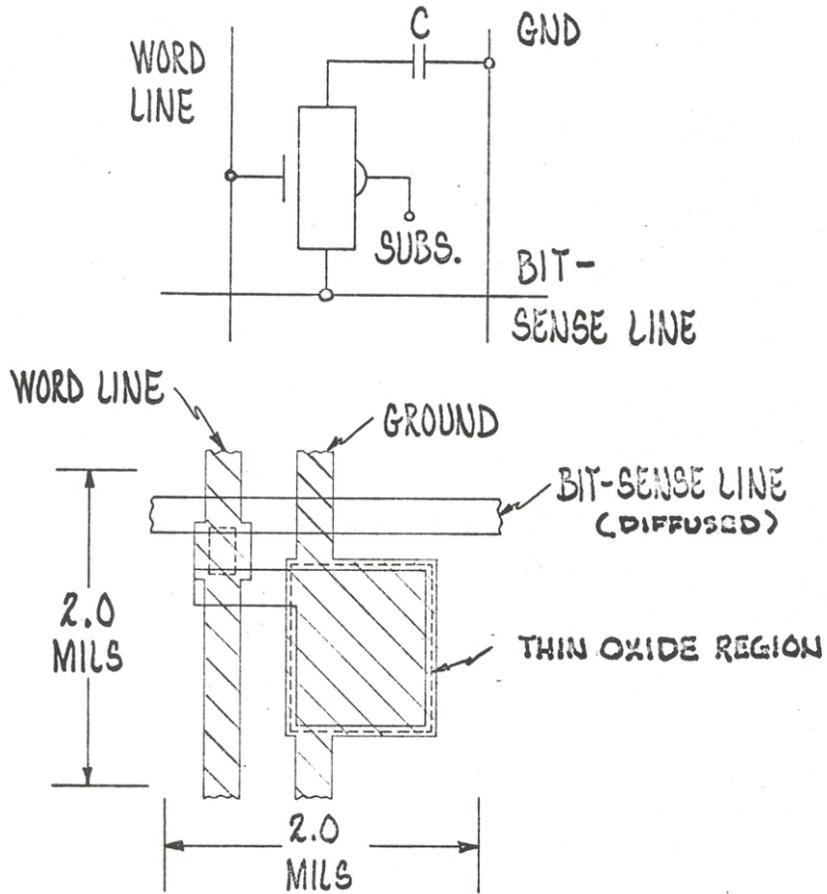


FIG. 2

June 4, 1968

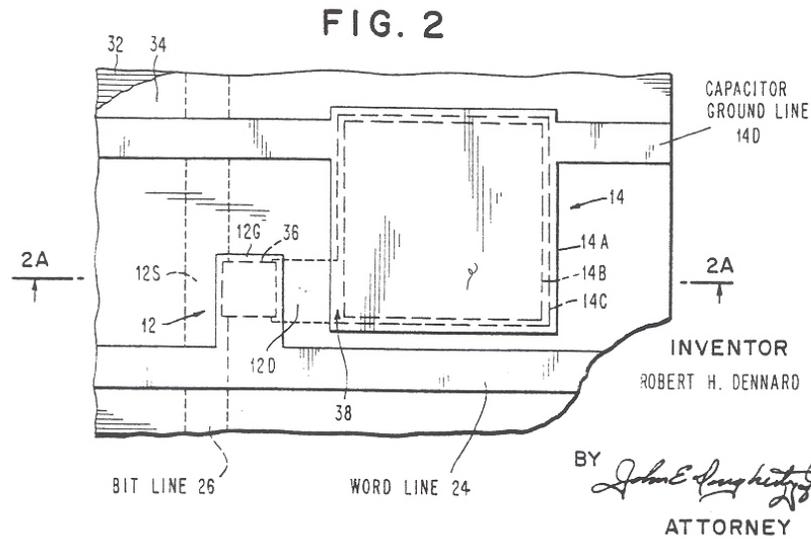
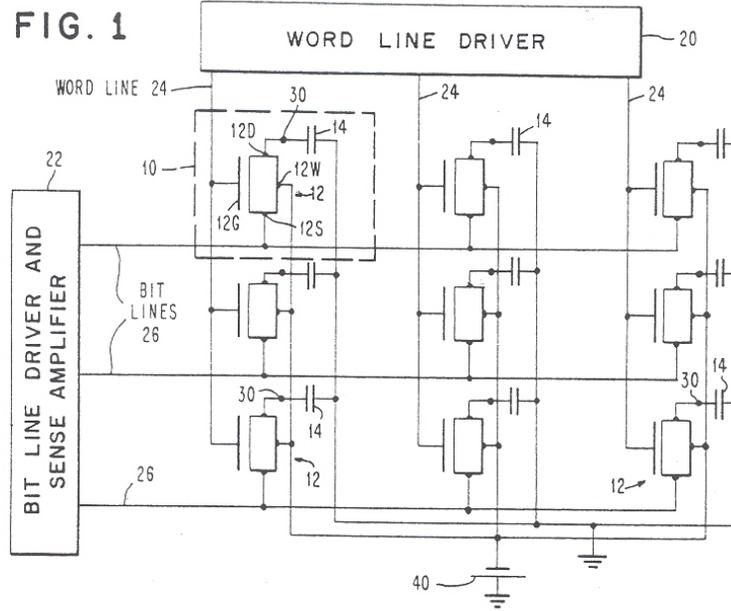
R. H. DENNARD

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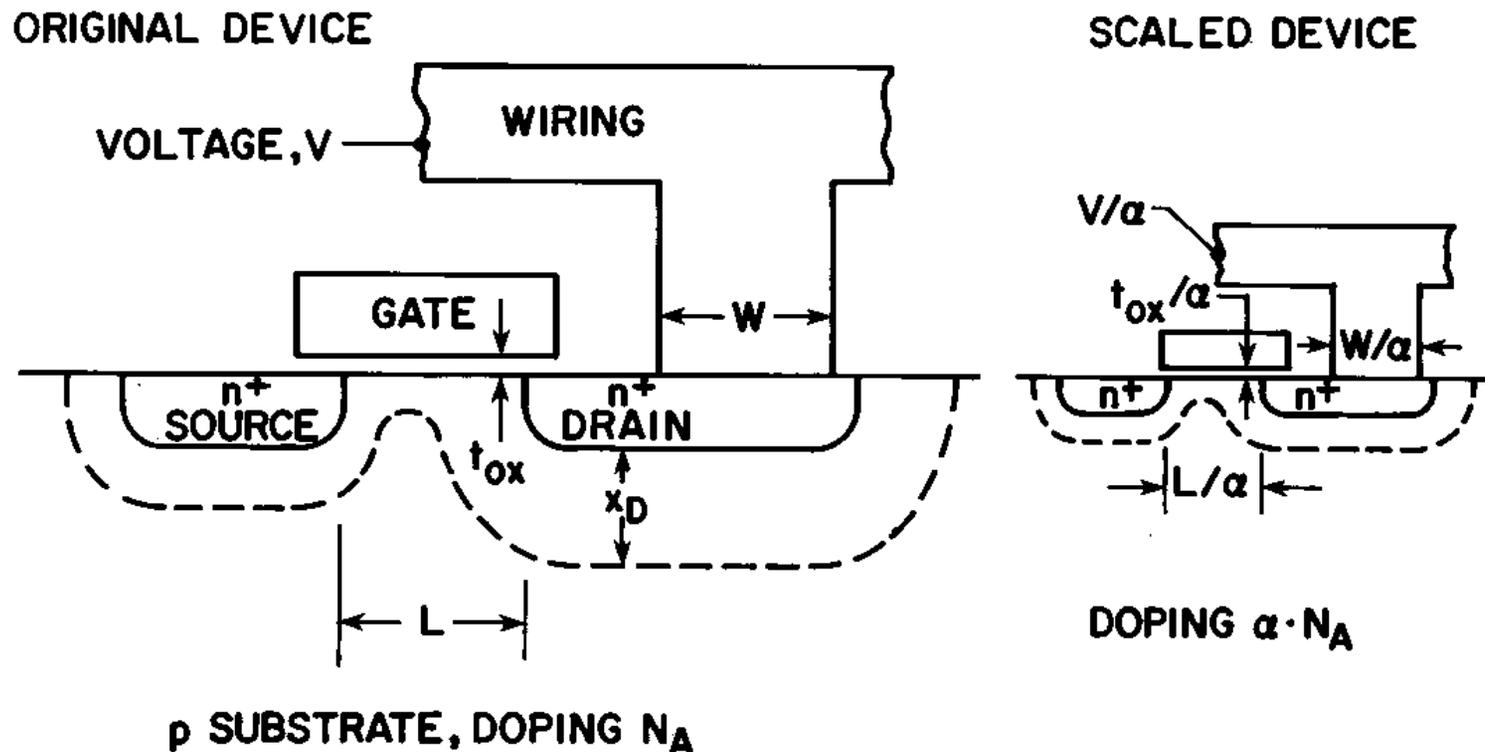
FIELD-EFFECT TRANSISTOR MEMORY

Filed July 14, 1967

3 Sheets-Sheet 1



Scaling Principles for MOS Technology



RESULTS:

Density increases by α^2 (wire)

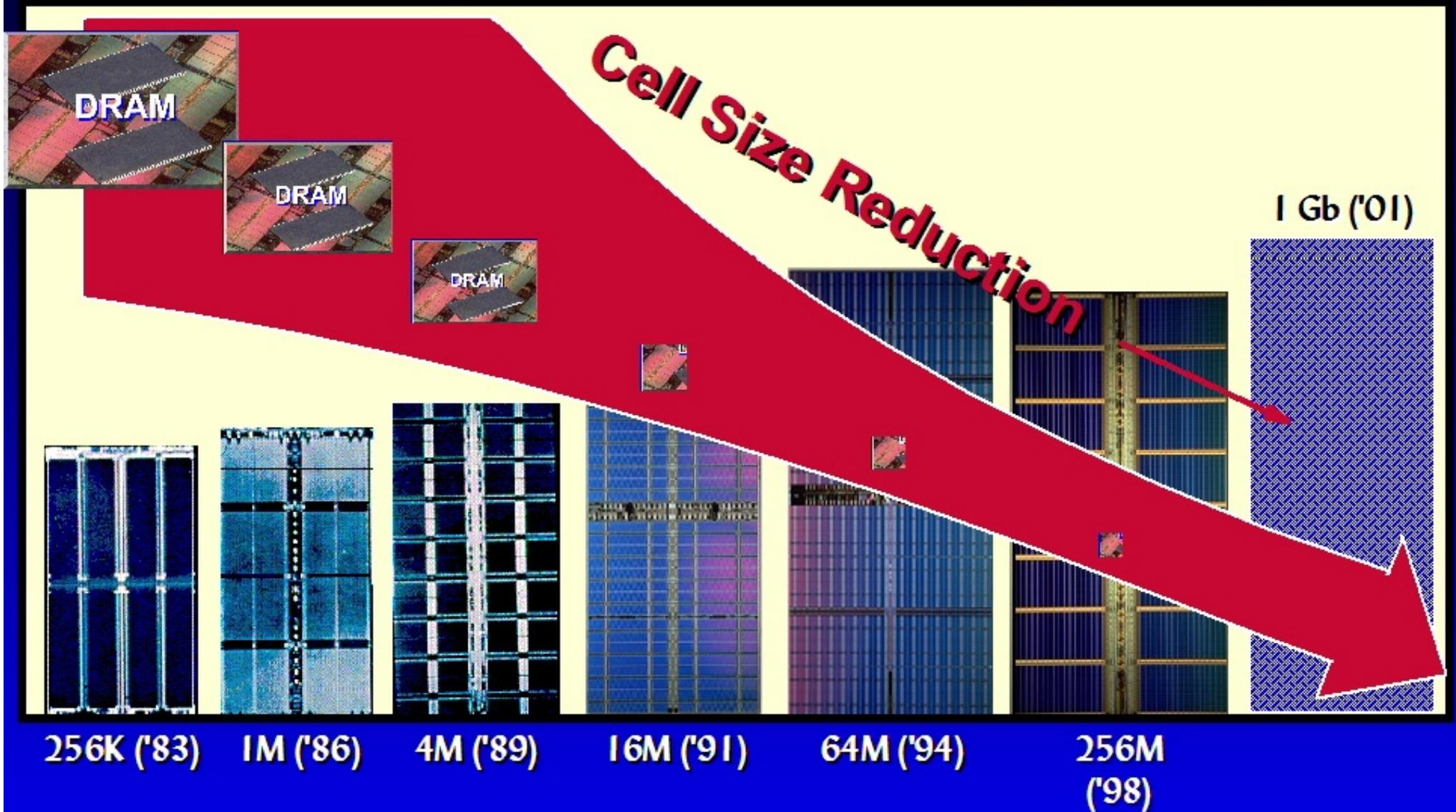
Speed increases by α (device)

Power/circuit decreases by α^2 (wire & voltage)

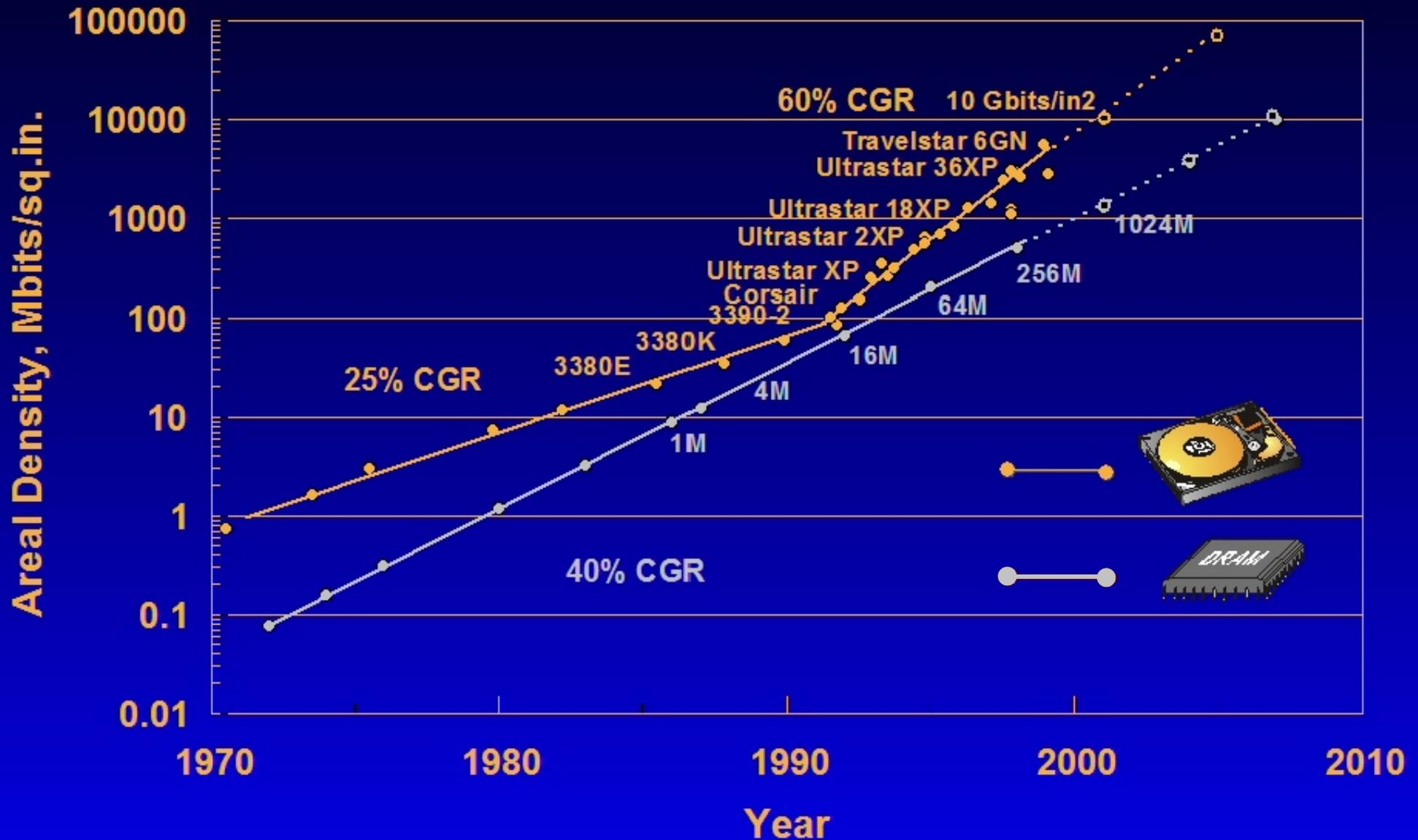
Wire RC unchanged by scaling

DRAM Evolution

- ◆ Bits/Chip Increase --- 4X/Gen. (~3 Years)



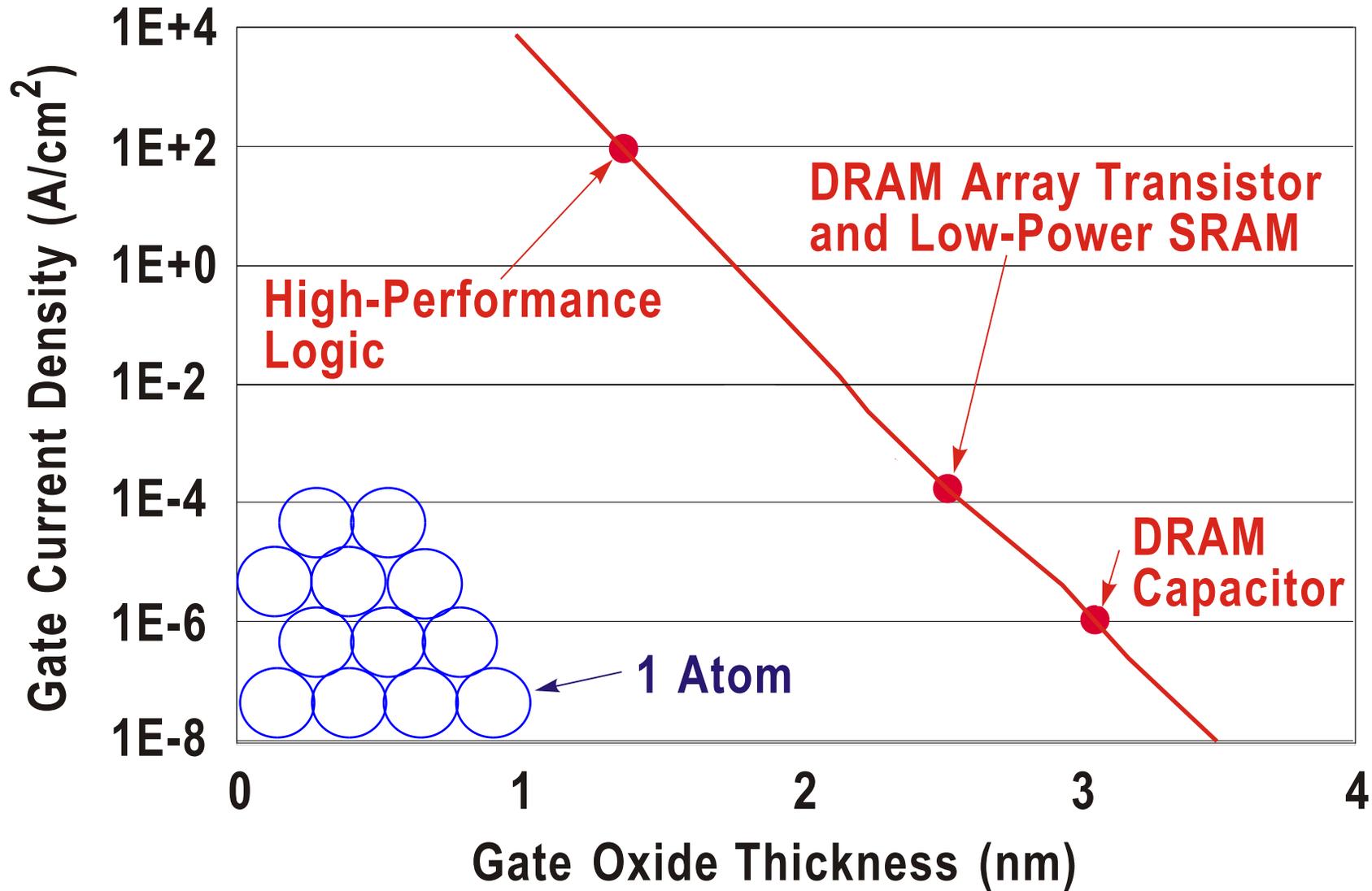
Areal Density of Magnetic HDD and DRAM



Future CMOS Technology Outlook – 45 nm and Beyond?

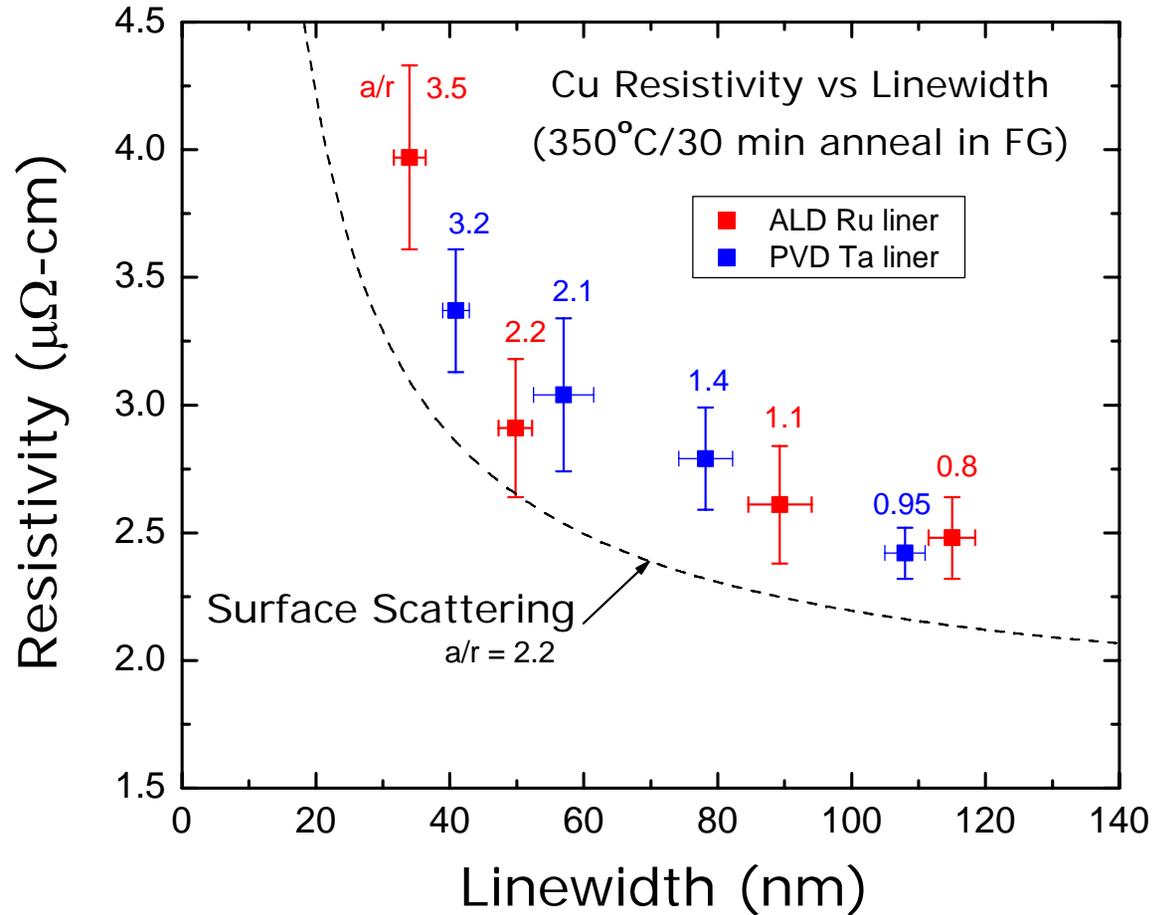
- **Transistor off-current limits voltage scaling**
 - lower voltage can be more energy efficient with lower performance
- **Gate-oxide tunneling limits conventional insulator scaling**
- **Increasing variability problems**
 - line edge control and roughness
 - doping fluctuations
 - soft errors (SER)
- **Strain engineering and surface orientation (HOT) for higher performance in near-term**
- **Several alternative structures for future**
 - challenging to build, incremental benefit in performance
 - needed to address variability problems

Limits of Oxide Scaling



(Gate voltage: 1.2V)

Wire Resistivity vs. Linewidth

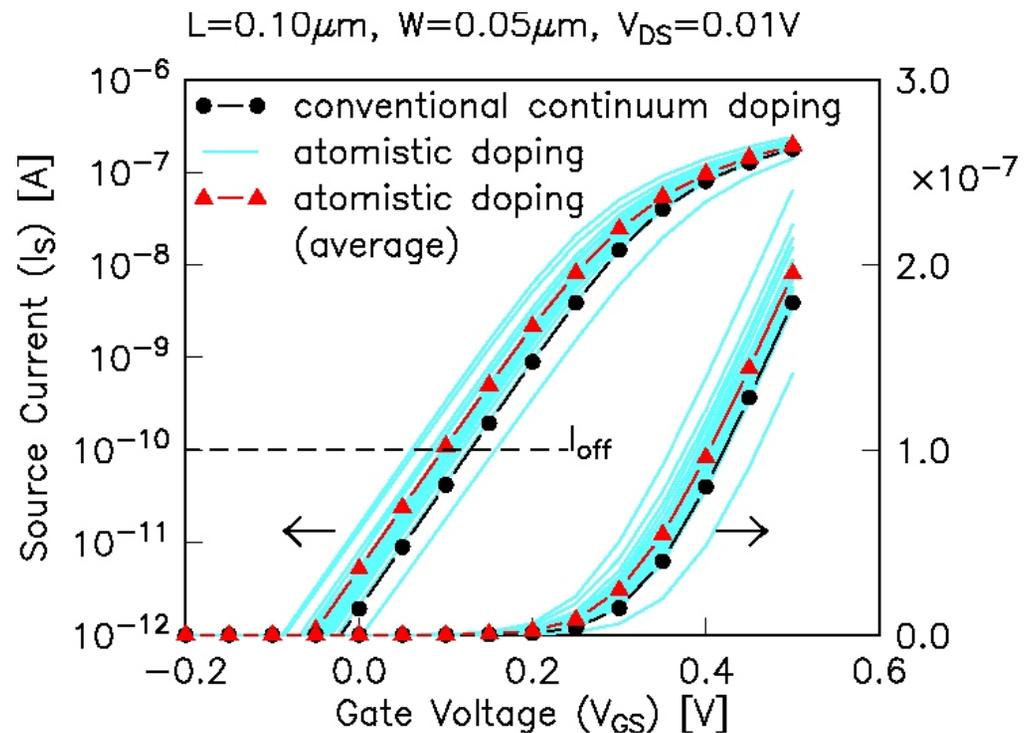
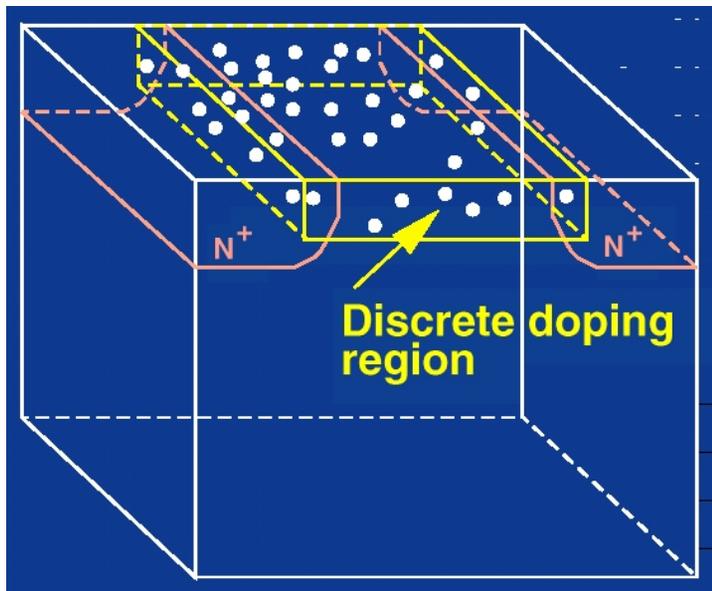


Discrete Random Dopant

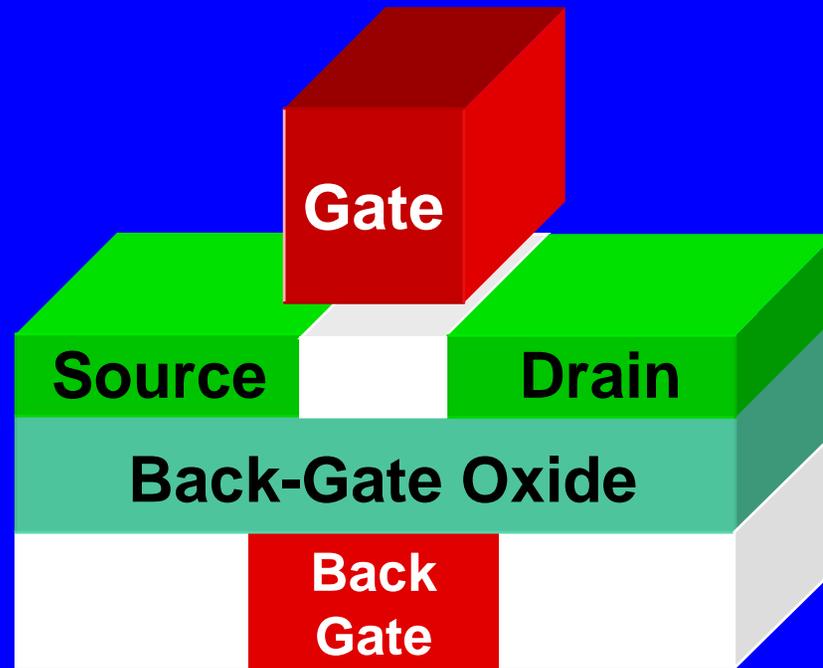
Number and location of individual dopant atoms:

- ◆ statistical fluctuations of I - V characteristics
- ◆ $\sim 10W^{-1/2} \text{ mV} \cdot \text{m}^{1/2}$ (W in m 's)

Solution: leave dopants out of channel



Back-Gate FET



- Undoped channel DG structure with thick back-gate oxide
- Back-gate tied to fixed DC potential
 - Creates vertical electric field, which confines inversion layer to top SOI surface and set V_T
 - Short-channel effects can be controlled with thicker T_{body} than UTB/DG
 - Back-gate potential supplements gate work function engineering

The Next Phase of Microelectronics- Technology Maturity

- **Device Performance Levels Off**
- **Circuit Density Fixed or Improving Slowly**
- **Costs Continue to Decrease for Some Time**
 - Stable process
 - Longer product life cycles
 - Focus on cost reduction in manufacturing, e.g. automation
- **Emphasis on System Level Performance**
 - Parallel to massively-parallel systems
 - Power dissipation becomes a major issue
 - Highly integrated functions on a chip

Changing Integration Strategy

Old

Processors:

Speed
Moderate Power



Short L
Lower Voltage
Multiple Wiring
Layers

DRAM:

Low Cost
Low Power



Cell Density
Sparse Support Circuits
- More bits/sense line
Cell Capacitance and
Voltage

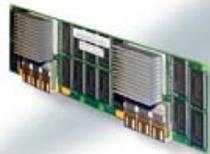
New

Merged Processor and DRAM:

- Processor based
 - lower-voltage, fast devices
 - less DRAM density
 - higher DRAM speed

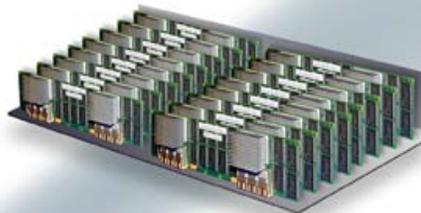
BlueGene/L System Buildup

Chip
2 Processors
2.8/5.6 GF/s
4 MB



5.6/11.2 GF/s
1.0 GB

Compute Card
2 Chips



90/180 GF/s
16 GB

Node Card
16 Compute Cards

Rack
32 Node Cards



2.8/5.6 TF/s
512 GB

System
64 Racks, 64x32x32 Chips



180/360 TF/s
32 TB

Conclusions

- **Scaling of Microelectronics Has Made Tremendous Progress in the Last Thirty-Five Years**
 - Many challenges have been met
- **Traditional Scaling May Slow Dramatically in This Decade**
 - Technology will evolve in other ways
- **Silicon Technology Will Reach a Very High Plateau**
 - Not easily challenged or replaced
- **Computing Power will Continue to Grow**
 - New applications will drive growth
 - Emphasis on design and energy efficiency